IN THE CLAIMS

What is claimed is:

1. A method comprising:

maintaining state information for a plurality of logical processors; and

applying the state information to a set of predefined rules to determine whether the logical processors can share a virtual address translation.

2. A method as recited in claim 1, wherein the state information includes a page table address associated with each of the logical processors.

3. A method as recited in claim 2, wherein said applying comprises determining whether the logical processors can share a virtual address translation based on a comparison of page table physical addresses.

4. A method as recited in claim 3, wherein said applying comprises determining that the logical processors can share a virtual address translation if page table physical addresses associated with the logical processors match.

5. A method comprising:

maintaining a plurality of page table addresses; and

determining whether the logical processors can share a virtual address translation based on the page table addresses.

6. A method as recited in claim 5, wherein each of the page table addresses corresponds to a page table of a different one of a plurality of logical processors, and wherein said determining comprises determining whether the logical processors can share a virtual address translation based on a comparison of page table addresses.

7. A method as recited in claim 6, wherein said determining comprises comparing an updated physical page table address with a physical page table address of each other logical processor of the plurality of logical processors.

8. A method as recited in claim 6, wherein said determining comprises determining that the logical processors can share a virtual address translation if page table addresses associated with the logical processors match.

9. A method as recited in claim 6, wherein said determining comprises determining that the logical processors can share a virtual address translation if physical page table addresses associated with the logical processors match.

10. A method as recited in claim 6, further comprising:

referring to the page table addresses using virtual page table addresses;

caching a plurality of physical page table addresses as translations of the virtual page table addresses; and

determining that the logical processors can share a virtual address translation if physical page table addresses associated with the logical processors match.

11. A method as recited in claim 10, further comprising updating at least one of the cached physical page table addresses in response to installing or deleting a translation for a base address of a page table.

12. A method as recited in claim 10, further comprising updating at least one of the cached physical page table addresses in response to performing a context switch.

13. An apparatus comprising:

means for maintaining state information for a plurality of logical processors; and

means for applying the state information to a set of predefined rules to determine whether the logical processors can share a virtual address translation.

14. An apparatus recited in claim 13, wherein the state information includes a page table address associated with each of the logical processors.

15. An apparatus recited in claim 14, wherein said means for applying comprises means for determining whether the logical processors can share a virtual address translation based on a comparison of page table physical addresses.

16. An apparatus recited in claim 15, wherein said means for applying comprises means for determining that the logical processors can share a virtual address translation if page table physical addresses associated with the logical processors match.

17. A multi-threaded processor comprising:

a plurality of logical processors; and

an address translation stage including

a translation lookaside buffer (TLB) to store a plurality of virtual address translations, and

a control logic to maintain a plurality of page table physical addresses, to compare an updated page table physical address to one of the plurality of page table physical addresses, and to determine whether two or more of a plurality of logical processors can share a virtual address translation based on an outcome of the comparison.

18. A multi-threaded processor as recited in claim 17, wherein the control logic updates a sharing indication in the TLB.

19. A multi-threaded processor as recited in claim 18, wherein the TLB controls access to a virtual address translation stored in the TLB based on the sharing status indication.

20. A multi-threaded processor as recited in claim 17, wherein the control logic includes one or more comparators to compare the updated page table physical address with a page table physical address of each other logical processor of the plurality of logical processors.

21. A multi-threaded processor as recited in claim 20, wherein the control logic generates an indication that the virtual address translation may be shared by the logical processors if the updated page table physical address matches each other page table physical address of the plurality of page table physical addresses.

22. A multi-threaded processor as recited in claim 20, further comprising a compare vector including a plurality of stored values, each value corresponding to a different one of the page table physical addresses, wherein the control logic causes each value to indicate whether the corresponding page table physical address matches the updated page table physical address.

23. A multi-threaded processor as recited in claim 22, wherein the control logic uses the compare vector to update a set of share vectors, each share vector corresponding to a different one of the logical processors, each share vector indicating the logical processors which can share virtual address translations.

24. A computing system comprising:

a plurality of logical processors;

a memory to store a plurality of virtual address translations; and

a control logic including

a comparator to compare a plurality of page table physical addresses with each other, each of the page table physical addresses associated with a different one of the logical processors, and

logic to generate an indication of whether the virtual address translations may be shared by the logical processors by generating an indication that the virtual address translations may be shared by the logical processors if the page table physical addresses match, and by generating an indication that the virtual address translations may not be shared by the logical processors if the page table physical addresses do not match.

25. A computing system as recited in claim 24, further comprising logic to install a virtual address translation in a translation lookaside buffer (TLB) based on the indication of whether the virtual address translations may be shared.

26. A computing system as recited in claim 24, further comprising logic to control access to a virtual address translation stored in a translation lookaside buffer (TLB) based on the sharing status indication.